

Response Times in Time-To-Live Caching Hierarchies under Random Network Delays

Karim Elsayed Joint work with Amr Rizk





















• Object admission to the cache is not instantaneous





• Aggregate requests during random fetching delays impact the performance







• Aggregate requests during random fetching delays impact the performance





• Extending an **exact** model of the caching hierarchy under **random network delays**



- Extending an **exact** model of the caching hierarchy under **random network delays**
 - Calculating the **exact** mean response time for cache hierarchies \rightarrow Importance?



- Extending an **exact** model of the caching hierarchy under **random network delays**
 - Calculating the **exact** mean response time for cache hierarchies \rightarrow Importance?
- Standing on the shoulders of
 - On the Impact of network delays on Time-to-Live caching [Elsayed]

[Elsayed] K. Elsayed, and A. Rizk, "On the Impact of Network Delays on Time-to-Live Caching," ArXiv abs/2201.1157, 2022.



- Extending an **exact** model of the caching hierarchy under **random network delays**
 - Calculating the **exact** mean response time for cache hierarchies \rightarrow Importance?
- Standing on the shoulders of
 - On the Impact of network delays on Time-to-Live caching [Elsayed]

[Elsayed] K. Elsayed, and A. Rizk, "On the Impact of Network Delays on Time-to-Live Caching," ArXiv abs/2201.1157, 2022.



- Extending an **exact** model of the caching hierarchy under **random network delays**
 - Calculating the **exact** mean response time for cache hierarchies \rightarrow Importance?
- Standing on the shoulders of
 - On the Impact of network delays on Time-to-Live caching [Elsayed]
 - Exact TTL Cache Hierarchy model under zero delay [Berger, Ciucu, 2014]

[Elsayed] K. Elsayed, and A. Rizk, "On the Impact of Network Delays on Time-to-Live Caching," *ArXiv abs/2201.1157, 2022.* [Berger] D. S. Berger et al. "Exact Analysis of TTL Cache Networks," *Performance Evaluation, vol. 79, pp. 2 – 23, 2014.*



TTL Cache Model

- Admission \rightarrow object is assigned a time to live (TTL)
- Eviction \rightarrow TTL expiration
- Hit \rightarrow TTL gets renewed



• Objects are decoupled in the cache



Cache Model

Markov arrival process

• A model for Markovian point processes





Cache Model

Markov arrival process

- A model for Markovian point processes
- Definition:



UNIVERSITÄT

D U I S B U R G E S S E N



- A model for Markovian point processes
- Definition:
 - $(D_0, D_1) \leftrightarrow$ (Hidden, Active) transition matrices
 - D_1 includes the transitions contributing to the **counting process**, where we count **misses**





- A model for Markovian point processes
- Definition:
 - $(D_0, D_1) \leftrightarrow$ (Hidden, Active) transition matrices
 - D_1 includes the transitions contributing to the **counting process**, where we count **misses**
- Model assumptions:



UNIVERSITÄT

DEUSEBURG



- A model for Markovian point processes
- Definition:
 - $(D_0, D_1) \leftrightarrow$ (Hidden, Active) transition matrices
 - D_1 includes the transitions contributing to the **counting process**, where we count **misses**
- Model assumptions:
 - Inter-request times, TTLs and delays are I.I.D, generally PH distributed



UNIVERSITÄT



- A model for Markovian point processes
- Definition:
 - $(D_0, D_1) \leftrightarrow$ (Hidden, Active) transition matrices
 - D_1 includes the transitions contributing to the **counting process**, where we count **misses**
- Model assumptions:
 - Inter-request times, TTLs and delays are I.I.D, generally PH distributed
 - TTLs can be random or deterministic



UNIVERSITÄT



- A model for Markovian point processes
- Definition:
 - $(D_0, D_1) \leftrightarrow$ (Hidden, Active) transition matrices
 - D_1 includes the transitions contributing to the **counting process**, where we count **misses**
- Model assumptions:
 - Inter-request times, TTLs and delays are I.I.D, generally PH distributed
 - TTLs can be random or deterministic
 - Tree-like cache hierarchy



UNIVERSITÄT



- A model for Markovian point processes
- Definition:
 - $(D_0, D_1) \leftrightarrow$ (Hidden, Active) transition matrices
 - D_1 includes the transitions contributing to the **counting process**, where we count **misses**
- Model assumptions:
 - Inter-request times, TTLs and delays are I.I.D, generally PH distributed
 - TTLs can be random or deterministic
 - Tree-like cache hierarchy
- Notation:



Cache Model

- A model for Markovian point processes
- Definition: •

The Ruhr Institute for Software Technology

- $(D_0, D_1) \leftrightarrow$ (Hidden, Active) transition matrices
- D_1 includes the transitions contributing to the **counting process**, where we count **misses**
- Model assumptions: ۲
 - Inter-request times, TTLs and delays are I.I.D, generally PH distributed
 - TTLs can be random or deterministic
 - Tree-like cache hierarchy



Our work:

M: exponentially distributed, PH: phase type, E: Erlang



Single M/M/M cache

- One object in/out of the cache is modelled using MAPs
- MAP has 3 states:
 - State "1": Object in the cache
 - State "0": Object out of the cache
 - State "F": Object being fetched



Active -----

- $1/\lambda$ mean inter-request time
- $1/\mu_F$ mean delay
- $1/\mu$ mean TTL



UNIVERSITÄT

DUISBURG ESSEN

- Goal: model the cache hierarchy using a total MAP
- Approach: **Exact recursive** superposition of single cache MAPs





UNIVERSITÄT

DUISBURG ESSEN



- Goal: model the cache hierarchy using a total MAP
- Approach: **Exact recursive** superposition of single cache MAPs
- From leaf caches:







UNIVERSITÄT

- Goal: model the cache hierarchy using a total MAP
- Approach: **Exact recursive** superposition of single cache MAPs
- From leaf caches:





UNIVERSITÄT

DUISBURG ESSEN



- Goal: model the cache hierarchy using a total MAP
- Approach: **Exact recursive** superposition of single cache MAPs
- From leaf caches:





UNIVERSITÄT

DUISBURG ESSEN

- Goal: model the cache hierarchy using a total MAP
- Approach: **Exact recursive** superposition of single cache MAPs
- From leaf caches:
 - Level superposition of siblings
 - Line superposition of parent-children





UNIVERSITÄT





• Construction of a system MAP from individual MAPs



UNIVERSITÄT DUISBURG ESSEN Offen im Denken

- Construction of a system MAP from individual MAPs
- Based on the Kronecker sum of individual MAPs

 $M = M_1 \oplus M_2$ $(D_0, D_1) = (D_0^{(1)}, D_1^{(1)}) \oplus (D_0^{(2)}, D_1^{(2)})$



UNIVERSITÄT D_U I_S_B_U_R_G E_S_S_E_N Offen im Denken

- Construction of a system MAP from individual MAPs
- Based on the Kronecker sum of individual MAPs

 $M = M_1 \oplus M_2$ $(D_0, D_1) = (D_0^{(1)}, D_1^{(1)}) \oplus (D_0^{(2)}, D_1^{(2)})$

• All the combination of states with the corresponding transitions.



UNIVERSITÄT D_U I_S_B_U_R_G E_S_S_E_N Offen im Denken

- Construction of a system MAP from individual MAPs
- Based on the Kronecker sum of individual MAPs

 $M = M_1 \oplus M_2$ (D₀, D₁) = (D₀⁽¹⁾, D₁⁽¹⁾) \oplus (D₀⁽²⁾, D₁⁽²⁾)

• All the combination of states with the corresponding transitions.





- Construction of a system MAP from individual MAPs
- Based on the Kronecker sum of individual MAPs

 $M = M_1 \oplus M_2$ (D₀, D₁) = (D₀⁽¹⁾, D₁⁽¹⁾) \oplus (D₀⁽²⁾, D₁⁽²⁾)

• All the combination of states with the corresponding transitions.







- Construction of a system MAP from individual MAPs
- Based on the Kronecker sum of individual MAPs

 $M = M_1 \oplus M_2$ $(D_0, D_1) = (D_0^{(1)}, D_1^{(1)}) \oplus (D_0^{(2)}, D_1^{(2)})$

- All the combination of states with the corresponding transitions.
- Independent caches \rightarrow Level superposition









• Line superposition \rightarrow Dependent caches




- Line superposition \rightarrow Dependent caches
- Approach?







- Line superposition \rightarrow Dependent caches
- Approach?
 - Kronecker sum







UNIVERSITÄT

D U I S B U R G E S S E N

- Line superposition \rightarrow Dependent caches
- Approach?
 - Kronecker sum \rightarrow problems?







UNIVERSITÄT

DUISBURG ESSEN

- Line superposition \rightarrow Dependent caches
- Approach?
 - Kronecker sum \rightarrow problems?
 - e.g., "1F"→ Parent fetching while object in child cache







UNIVERSITÄT

DUISBURG ESSEN

Complexity

- Model complexity
 - Number of states of the final MAP grows exponentially with the number of caches in the tree.
- Approach to reduce model complexity (while still exact) [Elsayed]
 - Leverage the symmetric structure within the tree.
 - Lumping the equivalent states.

[Elsayed] K. Elsayed, and A. Rizk, "On the Impact of Network Delays on Time-to-Live Caching," ArXiv abs/2201.1157, 2022.



- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache



UNIVERSITÄT

D U I S B U R G E S S E N

- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:





UNIVERSITÄT

D U I S B U R G E S S E N

- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:





UNIVERSITÄT

DUISBURG ESSEN

- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:

• Hit \rightarrow zero delay





UNIVERSITÄT

DUISBURG ESSEN

- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:

- Hit \rightarrow zero delay
- Miss $\rightarrow 1/\mu_F$

 λ : request rate λ_M : miss rate $1/\mu_F$: mean fetching time δ : random delay

 λ_M

δ

С

λ



UNIVERSITÄT

DUISBURG ESSEN

- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:

- Hit \rightarrow zero delay
- Miss $\rightarrow 1/\mu_F$ $\bar{R} = P_{hit} E[\delta|hit] + P_{miss} E[\delta|miss]$





UNIVERSITÄT

DUISBURG ESSEN

- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:

• Hit \rightarrow zero delay

$$\begin{array}{c} \mathsf{Miss} \rightarrow \ 1/\mu_F \\ \bar{R} = P_{hit} E[\delta|hit] + P_{miss} E[\delta|miss] \\ 0 \\ \end{array}$$

 $\begin{array}{lll} \lambda: & \text{request rate} \\ \lambda_M: & \text{miss rate} \\ 1/\mu_F: & \text{mean fetching time} \\ \delta: & \text{random delay} \end{array}$

λ



UNIVERSITÄT

DUISBURG ESSEN

- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:

• Hit \rightarrow zero delay

• Miss
$$\rightarrow 1/\mu_{F}$$

 $\bar{R} = P_{hit} E[\delta|hit] + P_{miss} E[\delta|miss]$
 0
 $1/\mu_{F}$
 λ_{M}
 λ
 λ_{I} : request rate
 λ_{M} : miss rate
 $1/\mu_{F}$: mean fetching time
 δ : random delay



- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:

• Hit \rightarrow zero delay

• Miss
$$\rightarrow 1/\mu_{F}$$

 $\bar{R} = P_{hit} E[\delta|hit] + P_{miss} E[\delta|miss]$
 0
 λ_{M}
 λ_{M}



UNIVERSITÄT

D U I S B U R G E S S E N

- The mean response time \overline{R} depends on
 - The mean fetching delay
 - The average miss rate at each cache

Single M/M/M cache:

• Hit \rightarrow zero delay

• Miss
$$\rightarrow 1/\mu_F$$

 $\overline{R} = P_{hit} E[\delta|hit] + P_{miss} E[\delta|miss]$
 $0 \qquad \frac{\lambda_M}{\lambda} \qquad 1/\mu_F$
• How to calculate λ_M ?

 λ : request rate λ_M : miss rate $1/\mu_F$: mean fetching time δ : random delay

 λ_M

δ

С

λ



UNIVERSITÄT

DUISBURG ESSEN

Single cache miss rate

• From the MAP $\rightarrow D_1$ contains the active transitions

 $\lambda_{_M}$

С

λ





UNIVERSITÄT

DUISBURG ESSEN

Single cache miss rate

- From the MAP $\rightarrow D_1$ contains the active transitions
 - $\lambda_{M} = \pi D_{1} \mathbf{1},$ π : Steady state probability vector **1**: All ones vector





UNIVERSITÄT

D U I S B U R G E S S E N

Single cache miss rate

- From the MAP $\rightarrow D_1$ contains the active transitions
 - $\lambda_{M} = \pi D_{1} \mathbf{1},$ π : Steady state probability vector **1**: All ones vector

 λ_{M}

С

λ

• Exact mean response time

$$E[R] = \frac{\pi D_1 \mathbf{1}}{\lambda \mu_f}$$





UNIVERSITÄT

DUISBURG ESSEN

M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache







UNIVERSITÄT

D U I S B U R G E S S E N

M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache





M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache

$$\bar{R} = \frac{\lambda_{M,1} E[\delta_1]}{1}$$





UNIVERSITÄT

D U I S B U R G E S S E N

M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache

$$\bar{R} = \frac{\lambda_{M,1} E[\delta_1]}{1}$$

 $\lambda_{M,1} \rightarrow \text{MAP M}_1 \text{ modelling C}_1$





M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache

 $\lambda_{M,1} \rightarrow \text{MAP M}_1 \text{ modelling C}_1$





59

UNIVERSITÄT

DUISBURG ESSEN

M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache

 $\bar{R} = \frac{\lambda_{M,1} E[\delta_1] + \lambda_{M,2} E[\delta_2]}{E[\delta_2]}$

 $\lambda_{M,1} \rightarrow \text{MAP M}_1 \text{ modelling C}_1$ $\lambda_{M,2} \rightarrow \text{MAP M}_2 \text{ modelling C}_2$





UNIVERSITÄT

DUISBURG ESSEN

M/M/M Cache Hierarchy

UNIVERSITÄT DUISBURG ESSEN Offen im Denken

• Iterative accumulation of fetching delays due to the misses at each cache

 $\bar{R} = \frac{\lambda_{M,1} E[\delta_1] + \lambda_{M,2} E[\delta_2] + \lambda_{M,3} E[\delta_3]}{2}$

 $\lambda_{M,1} \rightarrow \text{MAP M}_1 \text{ modelling C}_1$ $\lambda_{M,2} \rightarrow \text{MAP M}_2 \text{ modelling C}_2$





M/M/M Cache Hierarchy

Offen im Denken

UNIVERSITÄT

DUISBURG ESSEN

• Iterative accumulation of fetching delays due to the misses at each cache

 $\bar{R} = \frac{\lambda_{M,1} E[\delta_1] + \lambda_{M,2} E[\delta_2] + \lambda_{M,3} E[\delta_3]}{k_{M,3} E[\delta_3]}$

 $\lambda_{M,1} \rightarrow \text{MAP M}_1 \text{ modelling C}_1$ $\lambda_{M,2} \rightarrow \text{MAP M}_2 \text{ modelling C}_2$ $\lambda_{M,3} \rightarrow \text{MAP M modelling the tree}$





M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache

$$\bar{R} = \frac{\lambda_{M,1} E[\delta_1] + \lambda_{M,2} E[\delta_2] + \lambda_{M,3} E[\delta_3]}{\lambda_1 + \lambda_2}$$

 $\lambda_{M,1} \rightarrow MAP M_1 \text{ modelling C}_1$

$$\lambda_{M,2} \rightarrow MAP M_2 \text{ modelling } C_2$$

 $\lambda_{M,3} \rightarrow MAP M$ modelling the tree







M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache

 $\bar{R} = \frac{\lambda_{M,1} E[\delta_1] + \lambda_{M,2} E[\delta_2] + \lambda_{M,3} E[\delta_3]}{\lambda_1 + \lambda_2}$

 $\lambda_{M,1} \rightarrow \text{MAP M}_1 \text{ modelling C}_1$ $\lambda_{M,2} \rightarrow \text{MAP M}_2 \text{ modelling C}_2$

 $\lambda_{M,3} \rightarrow MAP M$ modelling the tree

• For any number of caches:





M/M/M Cache Hierarchy

• Iterative accumulation of fetching delays due to the misses at each cache

 $\bar{R} = \frac{\lambda_{M,1} E[\delta_1] + \lambda_{M,2} E[\delta_2] + \lambda_{M,3} E[\delta_3]}{\lambda_1 + \lambda_2}$

 $\lambda_{M,1} \rightarrow \text{MAP M}_1 \text{ modelling C}_1$ $\lambda_{M,2} \rightarrow \text{MAP M}_2 \text{ modelling C}_2$ $\lambda_{M,3} \rightarrow \text{MAP M modelling the tree}$

• For any number of caches:

$$\overline{R} = \frac{\sum_{i} \boldsymbol{\pi}^{i} \boldsymbol{D}_{1}^{i} \boldsymbol{E}[\delta_{i}] \boldsymbol{1}}{\sum_{i} \lambda_{i}}$$





PH fetching delay

• The fetching process is represented by multiple states





PH fetching delay

- The fetching process is represented by multiple states
 - Example: Erlang-2 distribution





PH fetching delay

- The fetching process is represented by multiple states
 - Example: Erlang-2 distribution







PH fetching delay

- The fetching process is represented by multiple states
 - Example: Erlang-2 distribution
- Aggregate requests see different mean delays







PH fetching delay

- The fetching process is represented by multiple states
 - Example: Erlang-2 distribution
- Aggregate requests see different mean delays
- Arrivals at states $[1, 0, F_1, F_2]$ see mean delays

 $\boldsymbol{\alpha} = [0, \frac{2}{\mu_F}, \frac{2}{\mu_F}, \frac{1}{\mu_F}]$







PH fetching delay

- The fetching process is represented by multiple states
 - Example: Erlang-2 distribution
- Aggregate requests see different mean delays
- Arrivals at states $[1, 0, F_1, F_2]$ see mean delays

 $\boldsymbol{\alpha} = [0, \frac{2}{\mu_F}, \frac{2}{\mu_F}, \frac{1}{\mu_F}]$







PH fetching delay

- The fetching process is represented by multiple states
 - Example: Erlang-2 distribution
- Aggregate requests see different mean delays
- Arrivals at states $[1, 0, F_1, F_2]$ see mean delays

 $\boldsymbol{\alpha} = [0, \frac{2}{\mu_F}, \frac{2}{\mu_F}, \frac{1}{\mu_F}]$

• For any fetching delay distribution

 $\bar{R} = \frac{\sum_{i} (\boldsymbol{\pi}^{i} \odot \boldsymbol{\alpha}) \boldsymbol{D}_{1}^{i} \boldsymbol{1}}{\sum_{i} \lambda_{i}}, \ \odot : \text{Hadamard prodcut}$

72


• Using the same concept we can calculate







- Using the same concept we can calculate
 - Mean response time for each input stream







- Using the same concept we can calculate
 - Mean response time for each input stream
 - Mean response time given a system hit/miss





- Using the same concept we can calculate
 - Mean response time for each input stream
 - Mean response time given a system hit/miss
 - Mean response time given a PH/PH/PH hierarchy







Evaluation

The Ruhr Institute for Software Technology

Delay impact on hit probability

- Two level M/M/M hierarchy
 - Simulation (only for validation)
 - MAP (Exact model)
 - Renewal approximation (based on Related work)



$ar{ au}_\Delta\;$ mean delay time / mean Inter-request time

Trace from SNIA, 2011. "Storage Networking Industry Association's Input/Output Traces, Tools, and Analysis Technical Work Group". lotta.snia.org



Evaluation

Response time

- Two level M/ E_2 / E_2 hierarchy
 - Simulation (only for validation)
 - MAP (Exact model)





Conclusion & Future direction

- Fetching delays in cache hierarchies remarkably impact the performance (response time and hit probability)
- MAPs for cache hierarchies are formed recursively to provide an exact model with delays
- Mean response time is iteratively calculated from the MAP
- **Open topic:** The Response time distribution derivation given the MAP of a cache hierarchy



UNIVERSITÄT

D_U_I_S_B_U_R_G

Offen im Denken